UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/543,028	04/04/2000	Thomas Anthony Montgomery	200-0098	5383

7590 12/17/2003

Daniel H Bliss
Bliss McGlynn PC
2075 West Big Beaver Road
Suite 600
Troy, MI 48084

EXAMINER	
GARCIA OTERO, EDUARDO	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 12/17/2003

3

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/543,028	MONTGOMERY, THOMAS ANTHONY	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: METHOD OF DETERMINING A SWITCH SEQUENCE PLAN FOR AN ELECTRICAL SYSTEM
2. First named inventor is: MONTGOMERY
3. Claims 1-13 have been submitted, examined, and rejected.
4. US Application was filed on 4/4/00, and no earlier priority is claimed.

Index of Prior Art

5. **Reed** refers to US Patent 4,292,543.
6. **Stevenson** refers to Microsoft Project 98 Bible, by Nancy Stevenson and Elaine Marmel, by IDG Books, 1997, ISBN 0-7645-3155-7, pages 22, 53, 55, 57, 93, 95, 124, 151, 187, 224, 225.
7. **Olson** refers to US Patent 6,480,815.

Definitions

8. **Webster** refers to Webster's Third New International Dictionary, Merriam-Webster Inc, copyright 1993.

Specification-objections-informalities

9. The Specification is objected to because of the following informalities. Appropriate correction is required.
10. SEQUENTIAL. The specification is inconsistent. The term "sequential" is used properly at page 11 line 3: "sequential, that is closed one at a time", and is used properly in FIG 3 and FIG 4.
11. However, the term sequential is used improperly (and inconsistently) at page 3 line 3: "sequential group of switches to be closed together". The term sequential is also similarly used improperly in all independent claims: 1, 7 and 11.
12. COINCIDENT. Similarly, the term "coincident" is used inconsistently and improperly at the same locations as the term "sequential". See claim interpretation below for additional discussion.

35 USC § 112-Second Paragraph-indefinite claims

13. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. **Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. Claim 1 states "a **sequential** group of switches to be closed together or a **coincident** group of switches to be closed one at a time". Note that Webster defines "sequential" as "arranged in a sequence: SERIAL", and Webster defines "coincident" as "occupying the same space or time... CONTEMPORARY".

16. SEQUENTIAL. The specification is inconsistent. The term "sequential" is used properly at page 11 line 3: "sequential, that is closed one at a time". However, the term sequential is used improperly (and inconsistently) at page 3 line 3: "sequential group of switches to be closed together". The term sequential is also used improperly in all independent claims: 1, 7 and 11.

17. COINCIDENT. Similarly, the term "coincident" is used inconsistently and improperly at the above locations of the specification and claims.

18. Claims 2-13 are also rejected for the same reasons as claim 1.

Claim Interpretation

19. **The claim language is interpreted in light of the specification.** Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns,* 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

20. Claim 1 states "a **sequential** group of switches to be closed together or a **coincident** group of switches to be closed one at a time". Note that Webster defines "sequential" as "arranged in a sequence: SERIAL", and Webster defines "coincident" as "occupying the same space or time... CONTEMPORARY". Thus, it appears that the terms "sequential" switches should be closed one at a time (sequentially), and that "coincident" switches should be closed simultaneously.

21. Thus, claim 1 is interpreted as "a **coincident** group of switches to be closed together or a **sequential** group of switches to be closed one at a time". Note that Examiner's interpretation matches the specification page 11 lines 2-4, and matches the FIG 4 (note the horizontal axis for time), but is contrary to the definition found at specification page 3 lines 3-5.
22. The Examiner suggests that the claims, and the specification page 3 lines 3-5, and the abstract should be amended to be consistent with specification page 11 lines 2-4, and to be consistent with the Examiner's above interpretation of claim 1.

35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
24. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: Determining the scope and contents of the prior art. Ascertaining the differences between the prior art and the claims at issue. Resolving the level of ordinary skill in the pertinent art. Considering objective evidence present in the application indicating obviousness or nonobviousness.
25. **Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable.**
26. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reed in view of Stevenson and Olson.
27. Claim 1 is an independent "method" claim with 6 limitations, labeled by the Examiner for clarity.
28. [1]-**"identifying the switches for the electrical system"** is disclosed by Reed FIG 1 switches 6A-6P and loads 4A-4F, and column 1 line 48 "minimizing peak loading through the staged and controlled initiation of operation of devices which consume significant quantities of electrical energy". Note that Reed identifies the basic problem of peak loading, and identifies the basic solution as controlling the timing of switching the loads.
29. Reed does not disclose the additional limitations.

30. [2]-**"organizing the identified switches within a switch group by defining a sequential group of switches to be closed together or a coincident group of switches to be closed one at a time and by defining a duration of time the switches should be closed"** is disclosed by Stevenson. Coincident (or simultaneous) is disclosed by Stevenson page 53 FIG 3-7 "each task is the same length by default, and each begins on the project start date". Sequential (or series or consecutive) is disclosed by Stevenson page 93 "link a whole range of tasks to be consecutive". Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Similarly, see page 151 FIG 6-21. Note that page 57 states "when you move a summary task, its subtasks move with it." Thus, subtasks are grouped together into summary tasks. See page 55 FIG 3-9 "outline hierarchy".
31. [3]-**"organizing the switch group in a data tree structure for the switch sequence plan"** is disclosed by Stevenson page 22 FIG 2-3 "Gantt chart", and page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series, and page 55 FIG 3-9 "outline hierarchy". Note that page 57 states "when you move a summary task, its subtasks move with it." Note that a Gantt chart is almost identical in format to the instant specification FIG 4 (switches or tasks located in unique vertical position, and time indicated in horizontal axis). Note that the specification FIG 3 "data [tree] structure" is inherent in specification FIG 4, and similarly the data structure is inherent in a Gantt chart, such as the Stevenson page 22 FIG 2-3 and page 187 FIG 7-12. Note that this type of series and parallel logical grouping is well known to electrical engineers (for example series resistors are often grouped and treated as a single resistor).
32. [4]-**"traversing the data tree structure recursively to calculate opening and closing times for the switches within the switch sequence plan"** is performed automatically by Stevenson as the tasks are entered or modified, page 57 states "when you move a summary task, its subtasks move with it." Also see page 95 "four basic dependency relationships".
33. [5]-**"generating an [sic] simulation command for setting a position sequence of the switches from the opening and closing times for the switch sequence plan"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".

34. [6]-**"using the commands within the switch sequence plan to operatively control the switches in a simulation of the electrical system"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".
35. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Stevenson and Olson to modify Reed. One of ordinary skill in the art, beginning with Reed's basic circuit and power constraints, would be motivated to simplify the design by grouping sets of switches into logical units as series or coincident ("parallel") as disclosed by Stevenson. Note that this type of logical grouping (series or parallel) is common in engineering practice, for example series and parallel resistors.
36. Additionally, one of ordinary skill would be further motivated to simulate the circuit model in order to verify timing constraints and power constraints, as disclosed by Olson. Note that Stevenson's Project 98 software performs a similar "simulation" each time its parameters are changed, and identifies conflicts at page 93 FIG 4-15 "Multiple dependencies or a combination of dependencies and constraints can cause conflicts in timing". Similarly, Stevenson page 224-225 spots resource conflicts "You can use views or filters to help you identify resource overallocation problems... overallocated resources appear in red." Further note that Stevenson's "resources" are analogous to "peak loading" in Reed, and analogous to "power" constraints in Olson".
37. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable Reed in view of Stevenson and Olson.
38. Claims 2-6 depend directly from claim 1, with one additional limitation each.
39. In claim 2, **"selecting an individual switch or a group of switches from a list displayed on a video terminal of a computer system"** is disclosed by Stevenson page 57 "when you move a summary task, its subtasks move with it."
40. In claim 3, **"nesting sequential switch groups and coincident switch groups within a top level switch group"** is disclosed by Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel). Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series.

41. In claim 4, **"determining a duration of time between switch closings for a sequential switch group"** is disclosed by Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Also see Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel).
42. In claim 5, **"nesting lower level sequential switch groups or coincident switch groups within higher level sequential switch groups or coincident switch groups"** is disclosed by Stevenson page 124 FIG 5-18: group item 2 contains item 3 and item 6 in series, and item 3 contains item 4 and item 5 in series. Similarly, group item 2 contains item 3 and item 10 in series, and item 10 contains items 11 and 13 in parallel.
43. In claim 6, **"using the switch sequence plan to analyze an electrical load distribution of the electrical system"** is disclosed by Reed FIG 1 and FIG 2 and FIG 3.
44. MOTIVATION FOR DEPENDENT CLAIMS 2-6. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Stevenson and Olson to modify Reed. One of ordinary skill in the art, beginning with Reed's basic circuit and power constraints, would be motivated to simplify the design by grouping sets of switches into logical units as series or coincident ("parallel") as disclosed by Stevenson. Note that this type of logical grouping (series or parallel) is common in engineering practice, for example series and parallel resistors. Similarly, the model may be further simplified by organizing additional layers of hierarchy, per Stevenson's hierarchy.
45. Additionally, one of ordinary skill would be further motivated to simulate the circuit model in order to verify timing constraints and power constraints, as disclosed by Olson. Note that Stevenson's Project 98 software performs a similar "simulation" each time its parameters are changed, and identifies conflicts at page 93 FIG 4-15 "Multiple dependencies or a combination of dependencies and constraints can cause conflicts in timing". Similarly, Stevenson page 224-225 spots resource conflicts "You can use views or filters to help you identify resource overallocation problems... overallocated resources appear in red." Further note that Stevenson's "resources" are analogous to "peak loading" in Reed, and analogous to "power" constraints in Olson".

46. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable Reed in view of Stevenson and Olson.
47. Claim 7 is an independent "method" claim with 8 limitations, labeled by the Examiner for clarity.
48. [1]-**"identifying the switches from a circuit schematic of the electrical system"** is disclosed by Reed column 1 line 48 "minimizing peak loading through the staged and controlled initiation of operation of devices which consume significant quantities of electrical energy".
49. Reed does not disclose the additional limitations.
50. [2]-**"selecting an individual switch or a group of switches from a list displayed on a video terminal of a computer system"** is disclosed by Stevenson page 57 states "when you move a summary task, its subtasks move with it."
51. [3]-**"organizing the identified switches within a switch group by defining a sequential group of switches to be closed together or a coincident group of switches to be closed one at a time"** is disclosed by Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel). Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series.
52. [4]-**"defining a duration of time the switches in the sequential switch group or coincident switch group should be closed"** is disclosed by Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Also see Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel).
53. [5]-**"organizing the switch group in a data tree structure for the switch sequence plan"** is disclosed by Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel). Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series.
54. [6]-**"traversing the data tree structure recursively to calculate opening and closing times for the switches in the sequential switch group or coincident switch group for the**

switch sequence plan" is disclosed by Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel). Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Note that Stevenson recalculates all the times immediately as the structure is amended.

55. [7]-**"generating a simulation command for setting a position sequence of the switches from the opening and closing times for the switch sequence plan"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".

56. [8]-**"using the commands within the switch sequence plan to operatively control the switches in a simulation of the electrical system"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".

57. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Stevenson and Olson to modify Reed. One of ordinary skill in the art, beginning with Reed's basic circuit and power constraints, would be motivated to simplify the design by grouping sets of switches into logical units as series or coincident ("parallel") as disclosed by Stevenson. Note that this type of logical grouping (series or parallel) is common in engineering practice, for example series and parallel resistors. Then one of ordinary skill would be motivated to simulate the circuit model to verify timing constraints and power constraints, as disclosed by Olson. Note that Stevenson's Project 98 software performs a similar "simulation" each time its parameters are changed, and identifies conflicts at page 93 FIG 4-15 "Multiple dependencies or a combination of dependencies and constraints can cause conflicts in timing". Similarly, Stevenson page 224-225 spots resource conflicts "You can use views or filters to help you identify resource overallocation problems... overallocated resources appear in red." Further note that Stevenson's "resources" are analogous to "peak loading" in Reed, and analogous to "power" constraints in Olson".

58. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable Reed in view of Stevenson and Olson.

59. Claims 8-10 depend directly from claim 7, with one additional limitation each.

60. In claim 8, **"determining a duration of time between switch closings for a sequential switch group"** is disclosed by Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Also see Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel).
61. In claim 9, **"nesting lower level sequential switch groups or coincident switch groups within higher level sequential switch groups or coincident switch groups"** is disclosed by Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Also see Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel).
62. In claim 10, **"using the switch sequence plan to analyze an electrical load distribution of the electrical system"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".
63. MOTIVATION FOR DEPENDENT CLAIMS 8-10. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Stevenson and Olson to modify Reed. One of ordinary skill in the art, beginning with Reed's basic circuit and power constraints, would be motivated to simplify the design by grouping sets of switches into logical units as series or coincident ("parallel") as disclosed by Stevenson. Note that this type of logical grouping (series or parallel) is common in engineering practice, for example series and parallel resistors. Similarly, the model may be further simplified by organizing additional layers of hierarchy, per Stevenson's hierarchy.
64. Additionally, one of ordinary skill would be further motivated to simulate the circuit model in order to verify timing constraints and power constraints, as disclosed by Olson. Note that Stevenson's Project 98 software performs a similar "simulation" each time its parameters are changed, and identifies conflicts at page 93 FIG 4-15 "Multiple dependencies or a combination of dependencies and constraints can cause conflicts in timing". Similarly, Stevenson page 224-225 spots resource conflicts "You can use views or filters to help you identify resource overallocation problems... overallocated resources appear in red." Further

note that Stevenson's "resources" are analogous to "peak loading" in Reed, and analogous to "power" constraints in Olson".

65. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable Reed in view of Stevenson and Olson.
66. Claim 11 is an independent "method" claim with 8 limitations, labeled by the Examiner.
67. [1]-**"identifying the switches from a circuit schematic of the electrical system"** is disclosed by Reed column 1 line 48 "minimizing peak loading through the staged and controlled initiation of operation of devices which consume significant quantities of electrical energy".
68. Reed does not disclose the additional limitations.
69. [2]-**"selecting an individual switch or a group of switches from a list displayed on a video terminal of a computer system"** is disclosed by Stevenson page 57 states "when you move a summary task, its subtasks move with it."
70. [3]-**"organizing the identified switches within a switch group by nesting within each other a sequential group of switches to be closed together or a coincident group of switches to be closed one at a time"** is is disclosed by Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel). Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series.
71. [4]-**"defining a duration of time the switches in the sequential switch group or coincident switch group within the top level switch group should be closed"** is disclosed by Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Also see Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel).
72. [5]-**"organizing the switch group in a data tree structure for the switch sequence plan"** is disclosed by Stevenson page 22 FIG 2-3 "Gantt chart", and page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series, and page 55 FIG 3-9 "outline hierarchy". Note that page 57 states "when you move a summary task, its subtasks move with it." Note that a Gantt chart is almost identical in format to the instant specification FIG 4 (switches or

tasks located in unique vertical position, and time indicated in horizontal axis). Note that the specification FIG 3 "data [tree] structure" is inherent in specification FIG 4, and similarly the data structure is inherent in a Gantt chart, such as the Stevenson page 22 FIG 2-3 and page 187 FIG 7-12. Note that this type of series and parallel logical grouping is well known to electrical engineers (for example series resistors are often grouped and treated as a single resistor).

73. [6]-**"traversing the data tree structure recursively to calculate opening and closing times for the switches in the sequential switch group or coincident switch group within the top level switch group for the switch sequence plan"** is disclosed by Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel). Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Note that Stevenson recalculates all the times immediately as the structure is amended.
74. [7]-**"generating a simulation command for setting a position sequence of the switches from the opening and closing times for the switch sequence plan"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".
75. [8]-**"using the commands within the switch sequence plan to operatively control the switches in a simulation of the electrical system"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".
76. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Stevenson and Olson to modify Reed. One of ordinary skill in the art, beginning with Reed's basic circuit and power constraints, would be motivated to simplify the design by grouping sets of switches into logical units as series or coincident ("parallel") as disclosed by Stevenson. Note that this type of logical grouping (series or parallel) is common in engineering practice, for example series and parallel resistors. Then one of ordinary skill would be motivated to simulate the circuit model to verify timing constraints and power constraints, as disclosed by Olson. Note that Stevenson's Project 98 software performs a similar "simulation" each time its parameters are changed, and identifies conflicts at page 93 FIG 4-15 "Multiple dependencies or a combination of dependencies and constraints can cause conflicts in timing". Similarly, Stevenson page 224-225 spots resource

conflicts "You can use views or filters to help you identify resource overallocation problems... overallocated resources appear in red." Further note that Stevenson's "resources" are analogous to "peak loading" in Reed, and analogous to "power" constraints in Olson".

77. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable Reed in view of Stevenson and Olson.
78. Claims 12-13 depend directly from claim 11, with one additional limitation each.
79. In claim 12, **"determining a duration of time between switch closings for a sequential switch group"** is disclosed by Stevenson page 124 FIG 5-18: the top level is item 1, a subgroup is item 3 (containing items 4 and 5 in series), and another subgroup is item 10 (containing items 11 and 13 in parallel). Also see Stevenson page 187 FIG 7-12 with items 3 and 4 in parallel, and items 1 and 9 in series. Note that Stevenson recalculates all the times immediately as the structure is amended.
80. In claims 13, **"using the switch sequence plan to analyze an electrical load distribution of the electrical system"** is disclosed by Olson FIG 14 "RUN SIMULATION" and "POWER ANALYSIS".
81. MOTIVATION FOR DEPENDENT CLAIMS 12-13. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use Stevenson and Olson to modify Reed. One of ordinary skill in the art, beginning with Reed's basic circuit and power constraints, would be motivated to simplify the design by grouping sets of switches into logical units as series or coincident ("parallel") as disclosed by Stevenson. Note that this type of logical grouping (series or parallel) is common in engineering practice, for example series and parallel resistors. Similarly, the model may be further simplified by organizing additional layers of hierarchy, per Stevenson's hierarchy.
82. Then one of ordinary skill would be motivated to simulate the circuit model to verify timing constraints and power constraints, as disclosed by Olson. Note that Stevenson's Project 98 software performs a similar "simulation" each time its parameters are changed, and identifies conflicts at page 93 FIG 4-15 "Multiple dependencies or a combination of dependencies and constraints can cause conflicts in timing". Similarly, Stevenson page 224-225 spots resource conflicts "You can use views or filters to help you identify resource overallocation

problems... overallocated resources appear in red." Further note that Stevenson's "resources" are analogous to "peak loading" in Reed, and analogous to "power" constraints in Olson".

Additional Cited Prior Art

83. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.

84. US Patent 6,080,201 by Hojat discloses Abstract "timing constraints... netlist... list of components", and column 1 line 31 simulation, and column 2 line 21 "power consumption", and column 2 line 57 "transistors" (note that transistors can act as switches), and column 2 line 67 "levels of hierarchy".

Conclusion

85. All claims stand rejected. The specification is objected to.

Communication

86. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER